REMARKS

Claims 1-16, 41-50, and 66-85 are pending in the application. The Applicants' attorney has amended claims 1, 6-9, 43-44, 68, 71-72, 74-76, 78-79, 81-82, and 84-85. As discussed below, the claims are in condition for allowance. **But if after considering this response the Examiner does not agree that all of the claims are allowable, he is respectfully requested to schedule and conduct a telephone interview with the Applicants' attorney before issuing a subsequent Office Action.**

Objections To The Specification

Contrary to the Examiner's rejection, the Applicants' attorney believes that the title as amended is descriptive. Therefore, the Examiner is asked to propose an amended title if he continues to believe that the current title is not descriptive. Or, alternatively, the Examiner is asked to table this objection until the Examiner allows the claims.

Claim Objections

The Applicants' attorney has amended claim 72 as proposed by the Examiner; therefore, the Applicants' attorney requests the Examiner to withdraw this objection.

Rejection Of Claims 1, 4-6, 41-42, 66, And 80 Under 35 U.S.C. § 102(b) As Being Anticipated By U.S. Patent 5,909,565 to Morikawa et al. ("Morikawa")

Claim 1

Claim 1 as amended, recites a hardwired-pipeline circuit operable to receive a message that includes data and that includes a header having information indicating a destination of the data by receiving the data and the information on at least one common bus line.

For example, referring, *e.g.*, to FIGS. 4-5 and paragraphs [57] and [97] – [100] of the patent application, in one embodiment, a pipeline circuit 80 (FIG. 4) has an input-data

handler 120 (FIG. 5) operable to receive via a pipeline bus 50 (see also FIG. 3) a message that includes data and that includes a header having information indicating a destination pipeline 74 for the data by receiving the data and information on at least one common line of the pipeline bus 50, to extract the data from the message, and to load the extracted data into a memory 92. An interface 140 is operable to retrieve the extracted data from the memory 92, and the destination pipeline 74 is operable to process the retrieved data.

In contrast, Morikawa does not disclose a hardwired-pipeline circuit operable to receive a message that includes data and that includes a header having information indicating a destination of the data by receiving the data and the information on at least one common bus line. Referring, *e.g.*, to FIG. 1 of Morikawa, a coprocessor 102 receives an instruction via a first bus (*i.e.,* a bus 126) and receives data via a second bus (*i.e.,* a bus 124). The data bus 124 carries only data, and thus does not carry information indicating a destination of the data. And, referring to Morikawa's FIG. 2, although Morikawa's instructions may include a form of data, the destination information within an instruction does not indicate a destination of the data included in the instruction, but instead indicates a destination of data resulting from an operation involving the data included in the instruction. Therefore, Morikawa's instruction bus 126 does not carry data and information indicating a destination of the carried data. Consequently, because no line of the data bus 124 carries information indicating a destination of the data carried by the data bus 124, and because no line of the bus 126 carries information indicating a destination of data included in an instruction, Morikawa discloses no common bus line that carries data and information indicating a destination of the data. Therefore, Morikawa's coprocessor 102 does not receive a message that includes data and that includes a header having information indicating a destination of the data by receiving the data and the information on at least one common bus line. Similar analyses apply to the other busses and to the coprocessors 202 (FIG. 4) and 302 (FIG. 10) of Morikawa.

Claims 4 and 5

These claims are patentable by virtue of their respective dependencies from claim 1.

Claim 6

Claim 6 as amended recites a processor operable to broadcast a message that includes data and that includes a header having information indicating a destination of the data, and a hardwired-pipeline circuit operable to receive the message from the processor by receiving the data and the information via at least one same bus line.

Therefore, claim 6 is patentable over Morikawa for reasons similar to those discussed above in support of the patentability of claim 1 over Morikawa.

Claim 41

Claim 41, as amended, recites receiving a message that includes data and that includes a header having information indicating a destination of the data and having information indicating a size of the message.

Morikawa does not disclose receiving a message that includes a header having information indicating a size of the message. Referring to sections 11 and 77 of the office action and to Morikawa's FIG. 2, the Examiner states that "the instruction opcode indicates an immediate value size (imm8, imm16, and imm32) of the message." The immediate values imm8, imm16, and imm32 are immediate data that are expanded and then multiplied by another number in the source register Dn to generate a result (col. 7, lines 35-40). Consequently, contrary to the Examiner's assertion, these immediate values do not indicate the size of the instruction opcode or of any portion the instruction opcode.

Claim 42

This claim is patentable by virtue of depending from claim 41.

Claim 66

This claim is patentable by virtue of depending from claim 1.

Claim 80

This claim is patentable by virtue of depending from claim 41.

Rejection Of Claims 1, 4, 41-42, 66, And 80 Under 35 U.S.C. § 102(b) As Being Anticipated By Hennessy and Patterson, "Computer Architecture – A Quantitative Approach, 2nd, Edition," 1996

Claim 1

Hennessy does not disclose a hardwired-pipeline circuit operable to receive a message that includes data and that includes a header having information indicating a destination of the data by receiving the data and the information on at least one common bus line. Referring to Hennessy's p. 155, a first instruction includes opcode LW, bits identifying a destination register R1, and, according to the Examiner, data B that the instruction LW causes to be loaded into R1. But referring to p. 134, this instruction is provided from an instruction memory on a bus IR, where each field LW, R1, and B of the instruction is carried by a respective group of bus lines. Therefore, even if the Examiner is correct that B is data and not an address of data, neither the ALU nor any other component in Hennessey's FIG. 3.4 receives the data B and the information R1 indicating a destination of the data on at least one common bus line; B and R1 are always carried by different bus lines.

Claim 4

Claim 4 is patentable by virtue of its dependency from claim 1.

Claim 41

Hennessy does not disclose receiving a message that includes data and that includes a header having information indicating a destination of the data and information indicating a size of the message. Referring to Hennessy's p. 155, contrary to the Examiner's position, the value B does not indicate a size of a message. First, B itself

cannot be a message, because it does not include information indicating a destination of itself (the Examiner's position is that B corresponds to "data" recited in claim 41). Second, according to the Examiner's position, B is a value to be loaded into the destination register R1. But even if the combination of B and R1 compose a message, there is no indication that B indicates the combined size of B and the binary value identifying R1.

Claim 42

This claim is patentable by virtue of depending from claim 41.

Claim 66

This claim is patentable by virtue of depending from claim 1.

Claim 80

This claim is patentable by virtue of depending from claim 41.

Rejection Of Claim 2 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Morikawa In View of U.S. 5,752,071 to Tubbs

Claim 2

Claim 2 is patentable by virtue of its dependency from claim 1.

Rejection Of Claims 3, 12, and 15 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Morikawa In View Of FOLDOC

Claim 3

This claim is patentable by virtue of its dependency from claim 1.

Claims 12 and 15

These claims are patentable by virtue of their dependencies from claim 9.

Rejection Of Claim 3 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Hennessy In View Of FOLDOC

Claim 3

This claim is patentable by virtue of its dependency from claim 1.

Rejection Of Claims 7-8, 43, 69-72, and 83-85 Under 35 U.S.C. § 103(a) As Being Unpatentable Over U.S. 4,985,832 To Gondalski

Claim 7

Claim 7 as amended recites a hardwired-pipeline circuit operable to process received data without executing a program instruction.

For example, referring to FIG. 4 of the patent application, a hardwired pipeline circuit 74 is operable to process data received from a data memory 92 without executing a program instruction.

In contrast, referring, e.g., to FIGS. 1-2, Gondalski discloses only processors 22 that process data by executing program instructions; consequently, Gondalski neither discloses nor suggests a hardwired-pipeline circuit operable to process received data without executing a program instruction.

Claims 69-70

These claims are patentable over Gondalski by virtue of their dependencies from claim 7.

Claim 8

This claim as amended is patentable over Gondalski for reasons similar to those recited above in support of the patentability of claim 7 over Gondalski.

Claim 43

This claim as amended is patentable over Gondalski for reasons similar to those recited above in support of the patentability of claim 7 over Gondalski.

Claim 83

This claim is patentable over Gondalski by virtue of its dependency from claim 43.

Claims 71-72 and 84-85

These claims as amended are patentable over Gondalski for reasons similar to those recited above in support of the patentability of claim 7 over Gondalski.

Rejection Of Claims 9-10, 44-45, 49, and 73 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Morikawa

Claim 9

Claim 9 as amended recites an output-data handler operable to generate a header having information indicating a destination of processed data, to generate a message that includes the processed data and the header, and to provide the message to an external source by providing the processed data and the information to the external source via at least one same bus line.

For example, referring, *e.g.*, to FIGS. 4-5 and paragraphs [57] and [102] – [104] of the patent application, in one embodiment, a pipeline circuit 80 (FIG. 4) has an output-data handler 126 (FIG. 5) operable to generate a header having information indicating a

destination of data processed by a hardwired pipeline 74, to generate a message that includes the processed data and the header, and to provide the message to an external source (e.g, another pipeline circuit 80) by providing the processed data and the information to the external source via at least one same bus line of the pipeline bus 50 (see also FIG. 3).

In contrast, Morikawa does not disclose or suggest an output-data handler operable to provide processed data and information indicating a destination of the processed data by providing the processed data and the information via at least one same bus line. Referring, *e.g.*, to FIG. 1 of Morikawa, a processor 101 provides to a coprocessor 102 an instruction via a first bus (*i.e.,* a bus 126) and data via a second bus (*i.e.,* a bus 124). The data bus 124 carries only data, and thus does not carry information indicating a destination of the data. And, referring to Morikawa's FIG. 2, although Morikawa's instructions may include a form of data, the destination information within an instruction does not indicate a destination of the data included in the instruction, but instead indicates a destination of data resulting from an operation involving the data included in the instruction. Therefore, Morikawa's instruction bus 126 does not carry data and information indicating a destination of the carried data. Consequently, because no line of the data bus 124 carries information indicating a destination of the data carried by the data bus 124, and because no line of the bus 126 carries information indicating a destination of data included in an instruction, Morikawa discloses no same bus line that carries data and information indicating a destination of the data. Therefore, Morikawa's processor 101 does not provide a message that includes data and that includes a header having information indicating a destination of the data by providing the data and the information on at least one same bus line, and there is no suggestion or motivation in Morikawa to modify the processor 101 and busses 124 and 126 to operate in the manner recited in claim 9. Similar analyses apply to the other busses and to the coprocessors 202 (FIG. 4) and 302 (FIG. 10) of Morikawa.

Claims 10 and 73

These claims are patentable by virtue of their dependencies from claim 9.

Claim 44

This claim as amended is patentable over Morikawa for reasons similar to those recited above in support of the patentability of claim 9 over Morikawa.

Claims 45 and 49

These claims are patentable by virtue of their dependencies from claim 44.

Rejection Of Claims 11 And 46 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Morikawa In View Of Fette

Claim 11

This claim is patentable over Morikawa in view of Fette by virtue of its dependency from claim 9.

Claim 46

This claim is patentable over Morikawa in view of Fette by virtue of its dependency from claim 44.

Rejection Of Claims 13-14 And 47-48 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Morikawa In View Of Frey

Claims 13-14

These claims are patentable over Morikawa in view of Frey by virtue of their dependencies from claim 9.

Claims 47-48

These claims are patentable over Morikawa in view of Frey by virtue of their dependencies from claim 44.

Rejection Of Claims 16 And 50 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Morikawa

Claim 16

This claim is patentable over Morikawa by virtue of its dependency from claim 9.

Claim 50

This claim is patentable over Morikawa by virtue of its dependency from claim 44.

Rejection Of Claims 1, 67-68, And 81-82 Under 35 U.S.C. § 103(a) As Being Unpatentable Over U.S. 5,377,333 to Nakagoshi

Claim 1

Claim 1 as amended recites a hardwired-pipeline circuit operable to process retrieved data without executing a program instruction.

For example, referring to FIG. 4 of the patent application, a hardwired pipeline circuit 74 is operable to retrieve data from a data memory 92 and to process the retrieved data without executing a program instruction.

In contrast, referring, e.g., to FIGS. 1 and 8, Nakagoshi discloses only computing clusters 103 that process data by executing program instructions; consequently, Nakagoshi neither discloses nor suggests a hardwired-pipeline circuit operable to process retreived data without executing a program instruction.

Claim 67

This claim is patentable over Nakagoshi by virtue of its dependency from claim 1.

Claims 68 and 81-82

These claims as amended are patentable over Nakagoshi for reasons similar to those recited above in support of the patentability of claim 1 over Nakagoshi.

Rejection Of Claims 74-79 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Nakagoshi In View Of Grandalski

Claim 74

Claim 74 as amended recites a hardwired-pipeline circuit comprising at least one hardwired pipeline operable to process data without executing a program instruction.

For example, referring to FIG. 4 of the patent application, a hardwired pipeline circuit 74 is operable to process data without executing a program instruction.

In contrast, as discussed above, Nakagoshi and Grondalski, viewed alone or in combination, fail to disclose or suggest a hardwired-pipeline circuit operable to process data without executing a program instruction.

Claims 75-76

These claims as amended are patentable over Nakagoshi in view of Grondalski for reasons similar to those recited above in support of the patentability of claim 74 over Nakagoshi in view of Grondalski.

Claim 77

This claim is patentable by virtue of its dependency from claim 76.

Claims 78-79

These claims as amended are patentable over Nakagoshi in view of Grondalski for reasons similar to those recited above in support of the patentability of claim 74 over Nakagoshi in view of Grondalski.

CONCLUSION

In view of the foregoing, claims 1-16, 41-50, and 66-85 are in condition for allowance. Therefore, the issuance of a formal Notice of Allowance at an early date is respectfully requested.

In the event additional fees are due as a result of this amendment, payment for those fees has been enclosed in the form of a check. Should further payment be required to cover such fees you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

DATED this 20th day of May, 2008.

Respectfully submitted,

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